Sheet <u>1</u> of <u>1</u>

FORM PTO-1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: FIS920000227US2	Divisional Application of U.S. Serial No.: 09/885,790
	FORMATION DISCLOSURE TATEMENT BY APPLICANT	APPLICANT: Divakaruni	et al.
(Use (37 CFR 1.98(b))	e several sheets if necessary)	FILING DATE:	PRIOR ART GROUP: 1765

REFERENCE DESIGNATION

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EXAMINER EXAMINER			U.S. PATENT DOCUMENTS				
	PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB- CLASS	FILING DATE II APPROPRIATE	
AA	5,895,253	04/20/1999	Akram				
AB	5,998,251	12/07/1999	Wu et al.				
AC	6,030,867	02/29/2000	Chien et al.				
AD	6,265,302	07/24/2001	Lim et al.				
AE	6,344,383	02/05/2002	Berry et al.				
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	AA AB AC AD AE AF AG AH AI	PATENT NUMBER AA 5,895,253 AB 5,998,251 AC 6,030,867 AD 6,265,302 AE 6,344,383 AF AG AH AI AI	PATENT NUMBER ISSUE DATE	PATENT NUMBER DATE PATENTEE	PATENT NUMBER DATE PATENTEE CLASS	PATENT NUMBER DATE PATENTEE CLASS SUB-CLASS	

FOREIGN PATENT DOCUMENTS

			PUBLICATION	COUNTRY OR		SUB-	TRANSI	ATION
		DOCUMENT NUMBER	DATE	PATENT OFFICE	CLASS	CLASS	YES	NO
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	AN				†			
	AO							
	AP		 		 			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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R	AQ	"A Novel Trench DRAM Cell with a <u>VERtIcal Access Transistor and BuriEd STrap</u> (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.				
PT	AR	"Extending Trench DRAM Technology to $0.15\mu m$ Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.				
P .	AS	"A 0.135 μ m ² 6F ² Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 780-81, IEEE, 2000.				
EXAMINE	R ()	DATE CONSIDERED 07/00/00				

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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